REMARKS

The application has been carefully reviewed in light of the Office Action dated August 21, 2003. Claims 88, 92-95, 97-121 and 123 are pending in the present application.

Claims 88, 92-95, 97-100, 105, 107-118 and 123 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Stone (U.S. Patent No. 5,770,476) in view of Jacobs et al. (U.S. Patent No. 4,811,082) in further view of Kumazawa et al. (U.S. Patent No. 5,569,960). Reconsideration and withdrawal of this rejection is respectfully requested.

Claim 88 recites, a process for forming an interposer element for use as a chip carrier comprising the steps of "providing an insulating layer on at least one surface of a silicon substrate" and "processing the insulating layer to produce at least one passive circuit element on or within the insulating layer, said at least one passive circuit element being separated from said silicon substrate by a portion of said insulating layer, said portion of the insulating layer having a thickness such that at least one passive circuit element is electrically shielded from the silicon substrate." Claim 88 further recites "solder bonding at least one integrated circuit chip to the interposer element, by forming a plurality of individual solder ball leads, wherein two or more of said individual solder ball leads use differing types of solder having differing melting points, such that at least one integrated circuit chip is electrically connected to at least one passive circuit element" and "forming a metallization pattern on or within the insulating layer, the metallization pattern being connected with said at least one passive circuit element."

This defined subject matter is not rendered obvious by the cited references. The device of Stone discloses an interposer that provides passive electronic components in circuit boards or cards. The device of Stone teaches the use of plated through holes 5 for electrically connecting components to various conductive planes. The Office Action acknowledges that Stone fails to teach or suggest an insulating layer on at least one silicon substrate; wherein the passive circuit element is being separated from the silicon substrate by a portion of the insulating layer; wherein two or more of the individual solder ball leads

use different types of solder having differing melting points, and a portion of the insulating layer having a thickness such that the passive circuit element is electrically shielded from the silicon substrate, as recited in claim 88. In order to overcome these numerous deficiencies in Stone, the Office Action relies on Jacobs.

The device of Jacobs discloses an integrated circuit packaging structure which provides high circuit density, high speed characteristics of wafer scale integration, reduced power requirements, discrete semiconductor segments, low electrical noise levels and thermal expansion matching between the discrete semiconductor segments and the substrate. The device of Jacobs has a reduced number of drivers and receivers for each semiconductor segment (32). The device of Jacobs utilizes solder balls that must be so small that the impedance between the internal circuits on the semiconductor segments 32 and the wiring of interposer 9 is substantially constant in order for an interposer to be used without receivers or drivers. The preferred size of the solder balls is 1-3 mils in diameter.

The Office Action further acknowledges that Stone and Jacobs fail to teach or suggest two or more individual solder ball leads which use differing types of solder having differing melting points. In order to overcome this deficiency, the Office Action relies on Kumazawa.

Kumazawa discloses an electronic component unit is provided with two electronic components which are disposed in parallel with each other and each of which has an internal electric circuit therein. Electrode pads are provided on the opposed surfaces of the two electronic components and are electrically connected to the internal electric circuits. The pads on one of the electronic components are respectively electrically and mechanically connected to the corresponding pads on the other electronic component by solder bumps. The device of Kumazawa has solder bumps of differing shape (from a spherical to hand drum shape) and electrode pads of differing size. The solder bumps used by the device of Kumazawa have a diameter of 0.6 mm. The solder bumps of differing shape and electrode pads of differing size are used to relieve stress to the outer portions of

substrates 3 and 9 due to thermal expansion as compared to central portions of substrates 3 and 9. Kumazawa fails to teach or suggest all the limitations of claim 88.

The Office Action fails to establish a *prima facie* case of obviousness of the subject matter of claim 88. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573 (Fed. Cir. 1996).

In the present case, the solder balls for Jacobs are on the order of 1-3 mils in diameter, and are required to be so small to keep the impedance constant between the internal circuits on the semiconductor segments and the wiring on the interposer, and reduce the lump capacitance of the interconnections, which is vital for allowing the use of an interposer without receivers or drivers. (See column 8 lines 9-18 and column 14 lines 47-50). The solder balls for Kumazawa have a diameter of 0.6 mm. The difference in size of the solder balls for Kumazawa are 8 to 24 times larger than those necessary for Jacobs. The solder balls for Stone are tangentially addressed as being applied using techniques known in the art. (See column 8 lines 49-52). There is no motivation to combine the references inherent in the references because an increase to the size of the solder balls for Jacobs would defeat the purpose of Jacobs of reducing the number of drivers and receivers of an integrated circuit structure.

The device of Jacobs has planar thin film capacitors integral with the package which decouple the power supply at individual vias 18 to any of the power planes in the package. (column 11 lines 56-58). In addition, the device of Jacobs requires that the power and signal feed-throughs 16, 24 described hereinafter are required because signals would normally attenuate when traveling through a metal via in a semiconductor body.

(See column 11 lines 7-13). There are no such requirements for the device of Kumazawa. To the contrary, in the device of Kumazawa, electrical signals are supplied from the semiconductor chip 1 to the electrodes of the substrate 3 through the wires 4 and reach lower electrode pads 6 through layered wiring in the substrate serving as conduction portions. The device of Jacobs teaches away from the signal connection method implemented by Kumazawa because Kumazawa sends electrical signals through a metal via in a semiconductor substrate without the use of feed throughs. The device of Stone also uses through holes and teaches away from the signal connection method of Kumazawa. (See FIG. 1). Because of the significant differences in structure and operation of the three cited references, there is no motivation for combining their teachings together.

Moreover, Stone, Jacobs and Kumazawa, whether considered alone or in combination, fail to teach or suggest a process for forming an interposer element for use as a chip carrier comprising the steps of "providing an insulating layer on at least one surface of a silicon substrate" and "processing the insulating layer to produce at least one passive circuit element on or within the insulating layer, said at least one passive circuit element being separated from said silicon substrate by a portion of said insulating layer, said portion of the insulating layer having a thickness such that at least one passive circuit element is electrically shielded from the silicon substrate." In addition, Stone, Jacobs and Kumazawa, whether considered alone or in combination, fail to teach or suggest "solder bonding at least one integrated circuit chip to the interposer element, by forming a plurality of individual solder ball leads, wherein two or more of said individual solder ball leads use differing types of solder having differing melting points, such that at least one integrated circuit chip is electrically connected to at least one passive circuit element" and "forming a metallization pattern on or within the insulating layer, the metallization pattern being connected with said at least one passive circuit element."

Therefore, Office Action fails to establish a *prima facie* case of obviousness because the Office Action fails to demonstrate (1), some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the references or combine the reference teachings, (2) a reasonable expectation of

success and (3) the prior art references must teach or suggest all claim limitations. Accordingly, the rejection of claim 88 should be withdrawn. Claims 92-95, 97-100, 105, 107-118 and 123 depend from claim 88 and are allowable over the combination of Stone, Jacobs and Kumazawa at least for the reasons mentioned above with respect to claim 88.

Claim 106 stands rejected under 35 U.S.C. 103(a) over Stone and Jacobs (and presumably Kumazawa; see rejection of claim 88) in further view of Yamazaki (U.S. Patent No. 6,002,161). Claims 101-104 stand rejected under 35 U.S.C. 103(a) over Stone and Jacobs in further view of Farooq et al. (U.S. Patent No. 5,912,044). Claims 119-121 stand rejected under 35 U.S.C. 103(a) over Stone, Jacobs and Yamazaki in further view of Solberg (U.S. Patent No. 6,121,676). Reconsideration and withdrawal of these rejections are respectfully requested.

Claims 101-104, 106, and 119-121 depend, directly or indirectly, from claim 88 and are allowable over Stone, Jacobs, Kumazawa, Yamazaki, Farooq and Solberg for the reasons mentioned above with respect to claim 88. Accordingly, the rejection of claims 101-104, 106, and 119-121 under 35 U.S.C. § 103(a) should be withdrawn. Moreover, there is no motivation for combining four or more references to attain the claimed invention.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By_____

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